Hybrid Solid State Disk Project

Guild lines for Internship

The School of Electrical Engineering and Computer Sciences (SEECS) is arranging a 6 weeks long internship program under the Hybrid Solid State Disk Project. The internship will provide students a platform to have hands on experience with the FPGAs and Verilog based hardware development.

The schedule along with the contents of the program is as follows:

General Information:

Duration: 6 Weeks
19th July -to- 28th August
Timings: 10 A.M -to- 4 P.M
Allocated Lab: Adv. Electronics Lab
(Fully available except for two hours on Wednesday and Thursday
Wednesday 10-11:50 AM
Thursday 2:20-4:10 PM)

Technical Specifications:

Software: Xilinx ISE 9.2 or 10.1
Hardware: Spartan 2 Kits

What to Bring

All the students will be required to bring a folder with them. This folder will contain attendance sheet, project guidance document, intermediate and final reports etc. This folder will be collected by us at the end.

Projects Offered

- Design and Implement of Delta sigma ADC on an FPGA board
- Design of good quality Band Pass Filter on FPGA and its Interface with network analyzer
- Design of good quality Low Pass Filter on
- FPGA and its Interface with network analyzer
- FPGA board Interface with LCD
- VGA interface FPGA board
- Keyboard and mouse interface with FPGA
- FGPA Interface with PC using Serial Port
- FPGA Interface with PC using LAN
- FPGA Interface with PC using PCIe
- FPGA Interface with GSM Module for sending SMS to mobile Phones
- Voice Encryption and Decryption using FGPA

Internship Certificate Requirements

- 80% Attendance is must.
- In addition to this certificate will be awarded to those who will be able to complete assigned tasks and projects within the specified time

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All the students will be required to handle FPGA kits very carefully as these are extremely costly (especially vertex5 kits). If students are found misusing/damaging these kits they will be required to repay the cost of the kit along with additional fine of Rs. 10,000.